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| Level | Type | Size | Latency | Description |
| Registers | GPR/FP | 16 +8 \* 32-bit | 1 cycle | Faster, holds operands |
| L1 I-Cache | Instruction | 8 KB | 1 cycle | Stores frequently used code |
| L1 D-Cache | Data | 8 KB | 1-2 cycles | Buffers data loads/stores |
| Scratchpad/TCM | On-chip RAM | 16 KB | 1 cycle | Deterministic acces for sensor |
| Main Memory(SRAM) | External RAM | 64 MB | 10-50 cycles | General data and program storage |
| Flash | Non-volatile | -- | 100 cycles | Firmware and logging |
| Peripherals | Memory-mapped | -- | Variable | Sensors, communication modules |